

Overview:

The DVB-S2 transmitter and receiver is an FPGA-based waveform implementing a fully compliant DVB-S2 Transmitter and Receiver chain per ETSI EN 302 307-1. The VHDL IP core is written in generic, synthesizable VHDL and is portable to any FPGA family. DVB-S2X (ETSI EN 302 307-2) extensions are supported as a future scope.

The transmitter and receiver designs are implemented on FPGA:

1. **Transmitter (Tx):** MPEG Transport Stream (188-byte) or Generic Stream (GS) input → Input Stream Synchronizer & Null-Packet Deletion → CRC-8 (BB Header) → BB Scrambler (PRBS/LFSR) → BCH Outer Encoder → LDPC Inner Encoder (rates 1/4–9/10, normal 64800-bit / short 16200-bit frame) → Bit Interleaver → QPSK/8PSK/16APSK/32APSK Bit Mapper → PL Framing + Pilot Insertion → PL Scrambler → SRRC BB Filter ($\alpha = 0.20/0.25/0.35$) → IQ Modulation → RF/Satellite. Max payload: 858 Mbits/s (8PSK, rate 9/10, Kintex UltraScale+ -2).
2. **Receiver (Rx):** ADC 16-bit IQ baseband input (sampling at $2 \times f_{clk_RXg}$) → DDC/NCO + AGC → SRRC Matched Filter ($\alpha = 0.20/0.25/0.35$, user programmable) → PLFRAME Detection & Sync → PL Descrambler → Auto Symbol Demod (QPSK/8PSK/16APSK/32APSK — auto-detected per frame) → Bit De-Interleaver → LDPC Decoder (LLR-based iterative) → BCH Decoder → BB Descrambler → Null-Packet Re-insertion → Output TS/GS. Max payload: >675 Mbits/s (8PSK, rate 9/10, Kintex UltraScale+ -2). FEC frame type, modulation and encoding rate auto-detected on a frame-to-frame basis.

Applications:

- Satellite Communication Ground Terminals — DVB-S2 Tx/Rx for ISRO, HAL, DRDO satellite TTC & payload data links (Ku-/Ka-Band)
- DVB-S2 Broadcast — direct-to-home (DTH) uplink/downlink, IP-over-satellite, broadcast video distribution
- Military SATCOM — QPSK/8PSK for LPI tactical satellite links; ACM for adaptive margin management under fading
- High-Throughput Satellite (HTS) — 16APSK/32APSK for broadband data (858 Mbps peak at Kintex UltraScale+)
- SIGINT / COMINT — wideband DVB-S2 signal intercept, modulation classification and replay (DRDO, DEAL)
- DVB-S2X extensions (ETSI EN 302 307-2) — higher-order APSK, ultra-low CNR modes for future HTS deployments

Key Specifications:

Parameters/Configurations	Supported Features
Inputs	-BBFRAMEs at the mode adaptation input interface. -Single or multiple MPEG Transport Stream. 188-Byte fixed length frames, Single or multiple Generic Stream (packetized or continuous).
Input stream synchronizer	Yes
Null packet deletion	Yes
Error correction encoding	LDPC + BCH
Encoding rate	1/4, 1/3, 2/5, 1/2, 3/5, 2/3, 3/4, 4/5, 5/6, 8/9, 9/10
Coding and modulation	CCM, VCM, ACM
FEC frame	normal (64800 bits) short (16200 bits)
Modulation	QPSK, 8-PSK, 16APSK, 32APSK
Maximum modulation symbol rate (Xilinx ultrascale+ -2 speed grade)	300 MSymbols/s 600 MSamples/s
RRC filter roll-off	0.35, 0.25 and 0.20
Output	complex (I,Q) baseband samples, 16-bit precision. DDR

Key Features of the System:

Transmitter (Tx) / Encoder & Modulator Chain:

- Flexible per-BBFRAME programmable attributes — frame length (16200/64800 bits), FEC encoding rate and modulation type can change dynamically every BBFRAME for VCM/ACM operation
- Input stream flexibility — Single/Multiple MPEG Transport Streams (188-byte), Generic Stream packetized or continuous, with input synchronizer, null-packet deletion and CRC-8 BB Header encoding
- Concatenated FEC — BCH outer code (n_{bch}, k_{bch}) + LDPC inner code (n_{dpc}, k_{dpc}); 11 code rates from 1/4 to 9/10; normal (64800-bit) and short (16200-bit) frame support
- QPSK/8PSK/16APSK/32APSK Gray-coded bit mapping with PLFRAME Header (MODCOD field) signalling; dummy PLFRAME insertion for continuous output
- PL Scrambler (BLER), Pilot Insertion (P=36 pilots per 1476-symbol period), SRRC BB filter ($\alpha = 0.20/0.25/0.35$) and quadrature modulation to 16-bit IQ DAC output

Receiver (Rx) / Demodulator & Decoder Chain:

- Automatic modulation detection on a frame-to-frame basis — QPSK, 8-PSK, 16APSK and 32APSK are identified from PLFRAME header without manual configuration
- Automatic encoding rate detection — all 11 rates (1/4 to 9/10) and both frame types (64800/16200 bits) auto-detected independently per PLFRAME
- LLR-based iterative LDPC decoder with BCH error correction; null-packet re-insertion and output TS/GS stream reconstruction with 188-byte packet alignment
- SRRC matched filter $\alpha = 0.20/0.25/0.35$ user programmable; input synchroniser and null-packet deletion on output side for transparent TS reconstruction
- ACM (Adaptive Coding & Modulation) controller — adjusts MODCOD per link margin via ACM COMMAND channel; VCM (Variable Coding) for multi-service streams
- Monitoring: Frame Error Rate, BER estimate, C/N ratio, SNR, EVM, signal quality; null-packet detection and CRC-8 check per BB frame
- Field-upgradeable via FPGA bitfile — LDPC rate, modulation order, rolloff and ACM policy updated without hardware change

Available Deliverables:

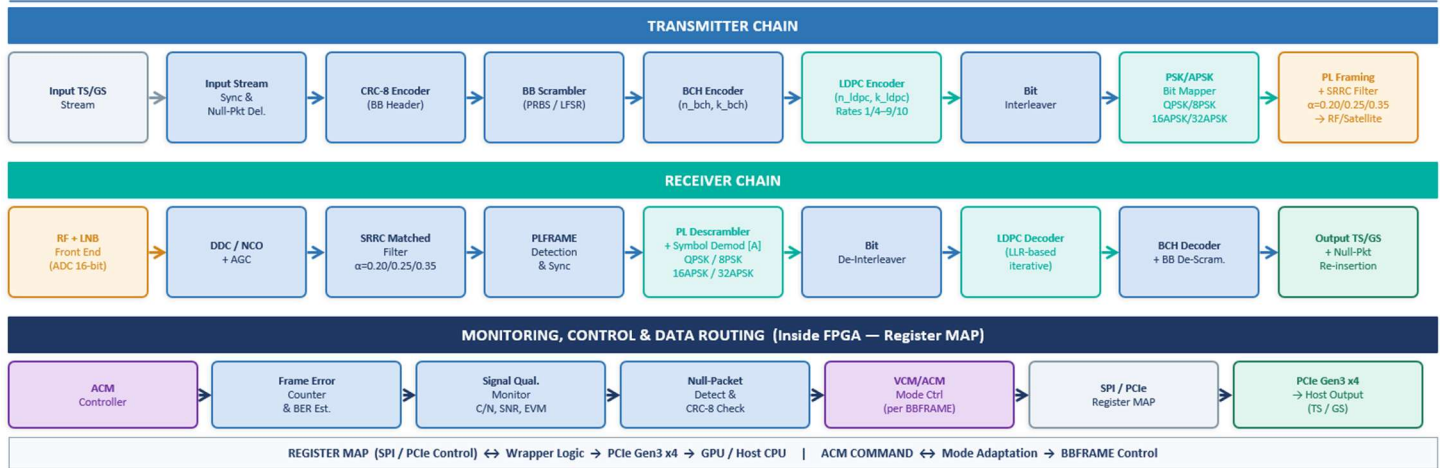
- FPGA bitfile + Register MAP: SPI/PCIe register map for all DVB-S2 Tx/Rx MODCOD and rolloff variants
- VHDL RTL Source Code/Netlist
- MATLAB/GNU Radio waveform generation (.m script/ .grc file) with PRBS11, AWGN; BER vs. E_b/N_0
- VHDL testbench + comprehensive datasheet and IP core interface specification

Reference documents:

- DVB-S2 specifications, ETSI EN 302 307-1 V1.4.1
- DVB-S2 Extensions (DVB-S2X) specifications ETSI EN 302 307-2 V1.1.1

Block Diagram:

Incise-DVB-S2 — System Block Diagram (DVB-S2 Tx / Rx Signal Processing Chain | ETSI EN 302 307-1)



[A] Modulation type, FEC rate & frame size auto-detected per PLFRAME (QPSK, 8-PSK, 16APSK, 32APSK) | LDPC: rates 1/4, 1/3, 2/5, 1/2, 3/5, 2/3, 3/4, 4/5, 5/6, 8/9, 9/10 | Incise Infotech Pvt. Ltd. - Incise TDL-DVB-S2 - CONFIDENTIAL