

Overview:

The PSK waveform is a software-defined radio (SDR) based waveform implementing both the transmitter and continuous-mode receiver for BPSK, QPSK, 8PSK and OQPSK modulations. The VHDL IP core is written in generic, synthesizable VHDL and is portable to any FPGA family.

The waveform is implemented on FPGA:

- 1. Transmitter (Tx):** Generates BPSK/QPSK/8PSK/OQPSK baseband IQ. Applies additive/multiplicative scrambling, bit-interleaving, FEC (RS/Turbo/LDPC), Gray-coded PSK symbol mapping, RRC pulse shaping (20/25/40 % rolloff selectable) and digital up-conversion.
- 2. Receiver (Rx):** Demodulator and Decoder chain with digital AGC, DDC/NCO, RRC matched filter (20/25/40 % rolloff), Costas PLL, Gardner symbol timing loop, AFC ($\pm 10\%$ acquisition), soft-quantised output and SNR/AGC/carrier-lock monitoring. Validated on Zynq UltraScale+ Evaluation Board (ZCU104) at 125 MHz.

Applications:

- Secure Combat-Net Radio (CNR) — BPSK/QPSK for robust Low Probability of Intercept (LPI) / Low Probability of Detection (LPD) tactical links
- Wideband SIGINT / COMINT — real-time intercept, classification and replay of BPSK/QPSK/8PSK/OQPSK signals across L/S/C-Band
- Airborne data-link for ALH-WSI / LCA Tejas — OQPSK for PA-efficient links; QPSK/8PSK for Ku/Ka-band satellite feeder
- DVB-S2 BPSK/QPSK satellite ground segment (ISRO TTC & payload downlink)
- Missile & UAV telemetry downlink (C-Band) — QPSK/8PSK for high-rate sensor payload
- EW jamming assessment & ECCM trials — runtime PSK mode switching under Register MAP control

Key Specifications:

Modulation	BPSK / QPSK / 8PSK / OQPSK (Runtime Configurable)
Spectral Efficiency	1 bps/Hz (BPSK) · 2 bps/Hz (QPSK/OQPSK) · 3 bps/Hz (8PSK)
Max Symbol Rate	fclk/4 (e.g. 31.25 MSymbols/s)
Throughput	Up to 120 Mbps (8PSK, Rate-3/4 LDPC, 40 MHz BW)
RRC Rolloff	20 % / 25 % / 40 % (selectable at build time)
Carrier Acq.	$\pm 1\%$ natural · $\pm 10\%$ AFC · $\pm 50\%$ extended
FEC	RS / Turbo Conv. / LDPC / Viterbi / Concatenated

Key Features of the System:

Transmitter (Tx) Chain:

- Runtime configurable PSK symbol mapping — single Register MAP write selects BPSK (Gray: 0/1), QPSK (Gray 2-bit), 8PSK (Gray 3-bit) or OQPSK (Q delayed $\frac{1}{2}$ symbol) with zero hardware change
- OQPSK mode offsets Q by $\frac{1}{2}$ symbol period, eliminating 180° phase transitions — reduces envelope fluctuation
- Differential encoding (DBPSK / DQPSK) option — conveys information in phase difference between successive symbols; resolves $n \times 90^\circ$ phase ambiguity without unique-word overhead
- Selectable RRC pulse-shaping filter: 20 %, 25 % or 40 % rolloff — firmware option selected at build time; limits spectral regrowth to allocated channel
- FEC transmit chain: additive/multiplicative LFSR scrambler → bit interleaver → RS outer code → Turbo/LDPC inner code — provides >4 dB net coding gain at BER = 10^{-6}

Receiver (Rx) / Demodulator & Decoder Chain:

- Digital AGC normalises input signal amplitude; outputs 4-bit soft-quantised samples (unsigned) or 8-bit signed format for internal carrier tracking loop processing
- 2nd-order Costas PLL carrier tracking loop — cancels average phase and frequency error; programmable loop gain ($x1/x2/x4/x8$) trades phase noise vs. thermal noise tolerance
- AFC (Automatic Frequency Control) loop extends initial acquisition to $\pm 10\%$ of symbol rate; extended circuit further reaches $\pm 50\%$ using spectrum symmetry. Must be disabled once locked to minimize implementation loss.
- Gardner symbol timing loop
- Wideband FFT IP Core (64–32K transform) for real-time spectrum analysis alongside demodulation — enables simultaneous signal monitoring without Rx disruption
- Comprehensive monitoring outputs: carrier lock indicator, frequency error, AGC gain, SNR estimate (averaged over 4096 symbols, <0.6 dB accuracy)
- Optional front-end: wider A/D sampling rate ($>8 \times$ symbol rate), IF under-sampling, CIC + half-band FIR decimation and bias removal

Available Deliverables:

- FPGA bitfile and Register MAP documentation — SPI/PCIe register map for all Tx/Rx PSK modes and RRC rolloff variants
- VHDL RTL source & all sub-components (Costas, AGC, Gardner, FFT, FEC)
- MATLAB Golden reference Models,
- VHDL test bench, product datasheet and IP core interface specification

Block Diagram

