QAM-16/32/64/128/256

Tactical SDR Waveform (Adaptive/Variable Coding & Modulation)

Overview:

Incise Tactical QAM waveform is a 100% indigenous software-defined radio (SDR) waveform purpose-built for tactical communication and intelligence applications in the Indian defense sector and other wireless domain applications.

The waveform is implemented on FPGA:

1. The FPGA hosts the QAM transmitter-receiver IP core, responsible for adaptive modulation (16/32/64/128/256-QAM), FEC encoding/decoding, and spectrum analysis via the Wideband FFT engine (64-32K transform).
2. The Transmitter-Receiver Chain is tested on Xilinx Zynq Ultrascale+ MPSoC based ZCU104 Evaluation Board, the decoded data is validated against the golden MATLAB reference model.

Applications:

- Combat-Net Radio (CNR) replacement for Network Centric Warfare/ Intelligence, surveillance and reconnaissance
- Wideband SIGINT / COMINT spectrum monitoring
- Airborne LOS data-link for Advanced Light Helicopter-Weapon Systems Integrated/ Light Combat Aircraft Tejas
- DVB-S2 + QAM hybrid satellite ground segment
- High-rate missile telemetry downlink (C-Band)
- EW (Electronic warfare) jamming assessment & ECCM (Electronic Counter-Counter Measures) waveform trials (Future Scope)

Key Specifications:

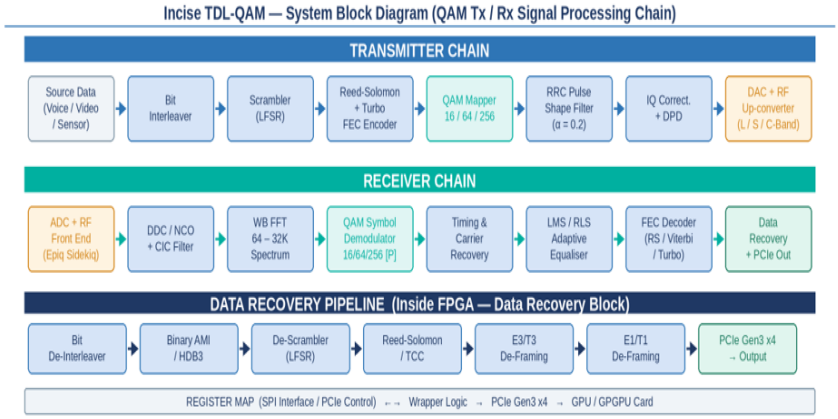
Modulation	**16/32/64/128/256-QAM (Adaptive/Variable)**
Throughput	Up to 200 Mbps
Bandwidth	5 / 10 / 20 / 40 MHz
FEC	Reed-Solomon/Turbo Convolutional Code/ LDPC/Viterbi/ Concatenated Codes
FFT	64 – 32K Transform
Output I/F	PCIe Gen3 x4

Key Features of the System:

- Adaptive 16/32/64/128/256-QAM modulation with Link Adaptation — up to 8 bps/Hz spectral efficiency
- High throughput: up to 200 Mbps raw data rate over 40 MHz channel bandwidth
- Wideband FFT IP Core (64-32K transform length) for real-time spectrum analysis alongside demodulation
- Uses Symbol Modulator/Demodulator (QAM 16-256), Equalizer, Convolutional Encoder, Additive/Multiplicative Scrambler, Interleaver, Viterbi/Reed-Solomon/TCC/LDPC Encoder-Decoder, De-Scrambler, Bit-Deinterleaver.
- Field-upgradeable waveform via FPGA Bit-Stream update — zero hardware change required
- Register MAP control via SPI and PCIe Gen3 x4 for real-time runtime parameter reconfiguration

Deliverables:

- FPGA bitfile and Register MAP documentation
- VHDL/Verilog RTL source for all IP cores (Symbol Demod, FFT, FEC, Data Recovery)
- MATLAB/Simulink baseband simulation model with BER curves
- Integration test bench and OTA loopback test procedure
- Comprehensive product datasheet and IP core interface specification



Block Diagram

Tx Chain: Source data is FEC-encoded (RS + Turbo), interleaved, scrambled, mapped to 16/64/256-QAM, RRC pulse-shaped and up-convertion.

Rx Chain: ADC samples are DDC/NCO down-converted, spectrum-analysed (WB FFT 64-32K), QAM-demodulated (Soft Symbol Demod), LMS/RLS equalised, and FEC-decoded.

Data Recovery: Bit de-interleaving, AMI/HDB3, de-scrambling, RS/TCC decoding inside the FPGA. Outputs via PCIe Gen3 x4 (DEMOD/FFT) under SPI/Register MAP.

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