Wideband Receiver Signal Processing System

Overview:

The architectural foundation of the Wideband Receiver Signal Processing System, outlines its two core components –

1. The FPGA component hosts the Wideband Demodulator & Decoder IP Core, which is responsible for receiving and processing IQ streams from RF cards through various stages, including demodulation and error correction. This hardware-accelerated processing is critical for handling high-speed data in real-time applications.
2. The GPGPU card complements the FPGA by executing C++ programs that configure the RF card for dynamic frequency hopping and manage the storage of processed data onto an SSD. This section emphasizes the synergy between these components, explaining how their combined capabilities enable the system to adapt to diverse operational requirements, making it a versatile solution for industries requiring reliable signal processing.

Application:

- High-Speed Space Communications (SatCom)
- Earth Observation and Remote Sensing
- Deep Space Network (DSN) Telemetry
- Space-Based Radar Systems
- Space Weather & Scientific Monitoring
- Electronic Warfare (EW) and SIGINT
- Interference Detection and Mitigation

Key Features of the system:

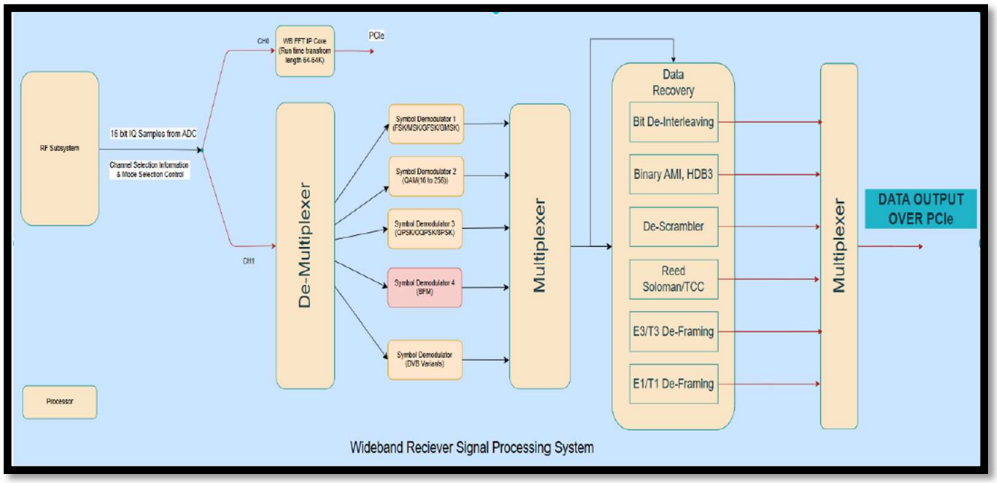
- Supports broad range of demodulation modes such as
  - DVB-S2X/S2/S, DVB-T2/T, DVB-H
  - FSK,
  - BFSK (upto 1Mbps)
  - MSK, GFSK,
  - GMSK,
  - BPSK,
  - QPSK,
  - 8PSK,
  - OQPSK, and
  - QAM (16, 32, 64, 128, 256),

  enabling compatibility with multiple communication standards.
- It also supports various line codes (Binary, AMI, HDB3, BnZS with n=3, 6, 8) and handles bit rates from 10 Kbps to 200 Mbps.
- The de-scrambler offers self/frame synchronized operation with standards like CCITT and V.35, featuring a 32-bit programmable design for custom PRN sequences.
- The channel decoder supports convolutional coding (k=7, rates 1/3 to 7/8), Reed-Solomon coding (GF(256, 285), k=6-255), and concatenated codes, along with de-interleaving options (2, 4, 8).
- The de-framing for E1, E3, T1, and T3 standards, and output of MPEG video and audio data, round out the feature set, making this IP core highly versatile.

Deliverables

- Tangible outputs provided with the system,
- VHDL/Verilog RTL code for FPGA implementation,
- Test benches for verification and
- A comprehensive datasheet.

This assures users of the complete package available for deployment and development.



Block Diagram

The diagram illustrates the routing of IQ streams from RF card channels through a switch to demodulation blocks (DVB, QAM, PSK, FSK, BFSK/BFM), with options for direct MPEG output or further processing via the Wideband FFT Core, bit de-interleaver, line decoder, descrambler, FEC decoder, and de-framing stages.

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